Semiconductor Solutions for 48V High Power Inverter

Alternatives to Bare Die Modules

Eric Schütte
Infineon Technologies AG

Agenda

1. High Power Inverters
2. Leadless SMD Packages
3. Bare Dies and MOSFET Modules
4. Innovative Packaging Concepts
5. Chip Embedding
6. Summary and Outlook

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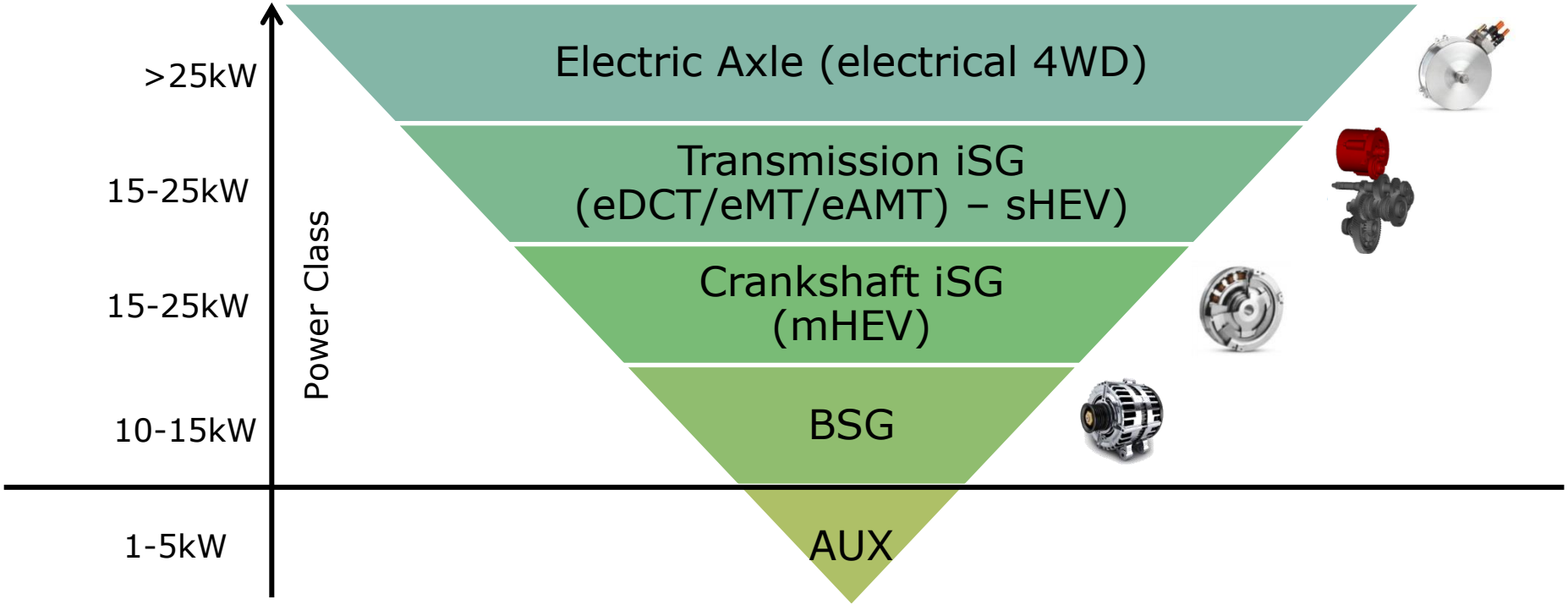
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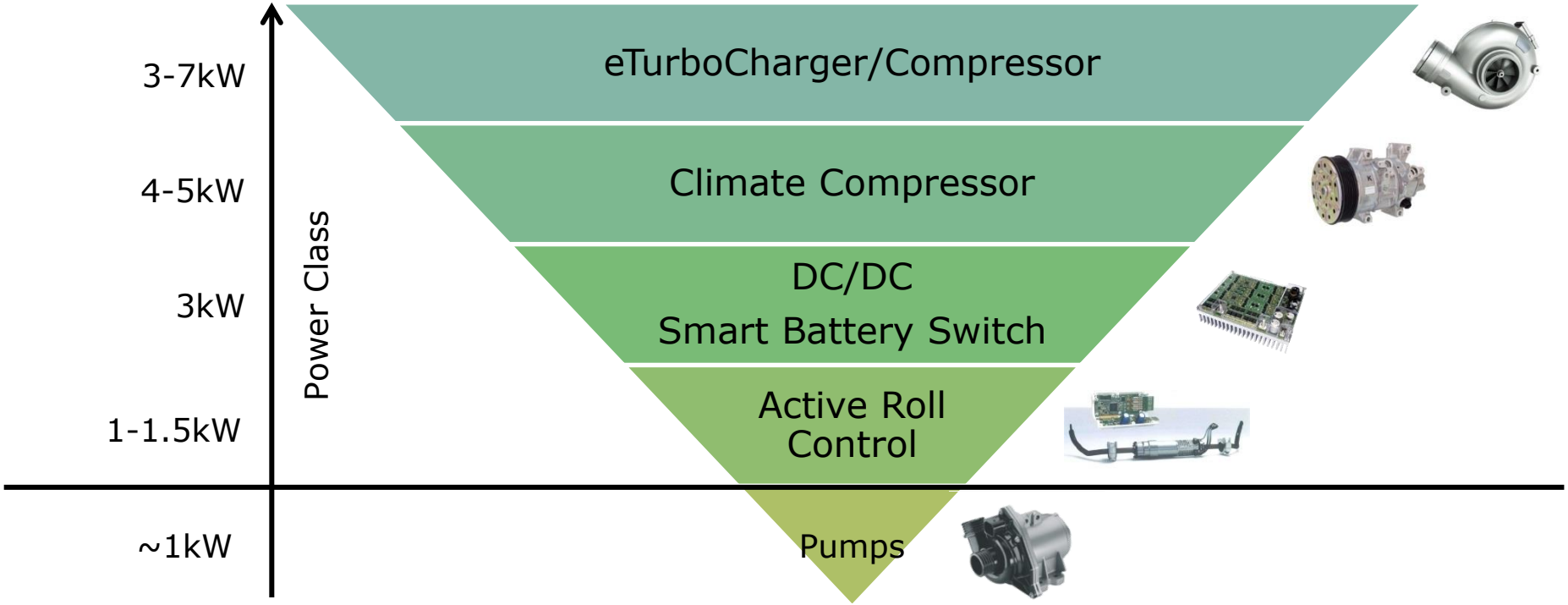
High Power Inverters
µHybridization

› Electrification and Hybridization



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High Power Inverters
Auxiliary Drives



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Agenda

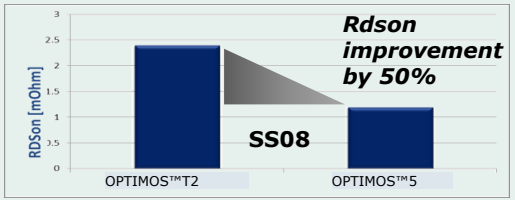
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Leadless MOSFETs
OptiMOS™5 80V/100V Trench Technology

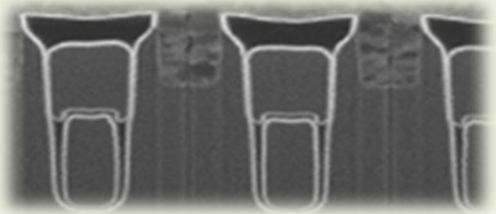
Best in Class Rdson

- Leading R_{DSon} performance down to 1.2mOhm (released)
- Low conduction losses
- Area reduction facilitates smaller packages



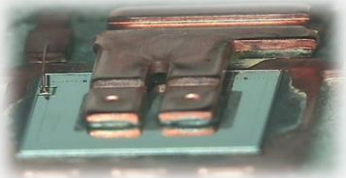
EMC Improvement

- Reduced Ciss & Coss
- Improved switching behavior
- Improved EMC behavior due to technology improvements



Innovative package interconnect

- New top-side copper-clip contact technology
- Lower thermal resistance
- Lower package resistance
- Smaller package e.g. Achieved a footprint 1/6th the size of a DPAK for equivalent R_{DSon}



1. Applicable to normal level

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Back End Technology Portfolio and Roadmap

SMD with cooling

Dual side cooling



DirectFET2 Large-CAN



DirectFET2 Medium-CAN



DirectFET2 Small-CAN

Lead-less SMD

Focussed for all new SFET Technologies



TOLL
TOLG



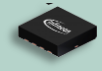
sTOLL7x8



…O8
…N5x6



Dual …N5x6
Dual S…

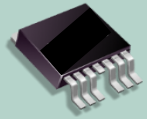


S3O8

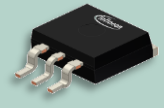
SMD with Leads



D2PAK-7P+



D2PAK-7



D2PAK



DPAK

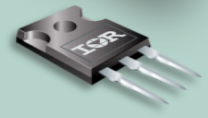


SO8

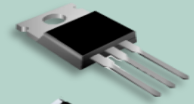
Through hole



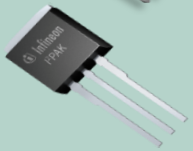
TO262WL



TO247



TO220



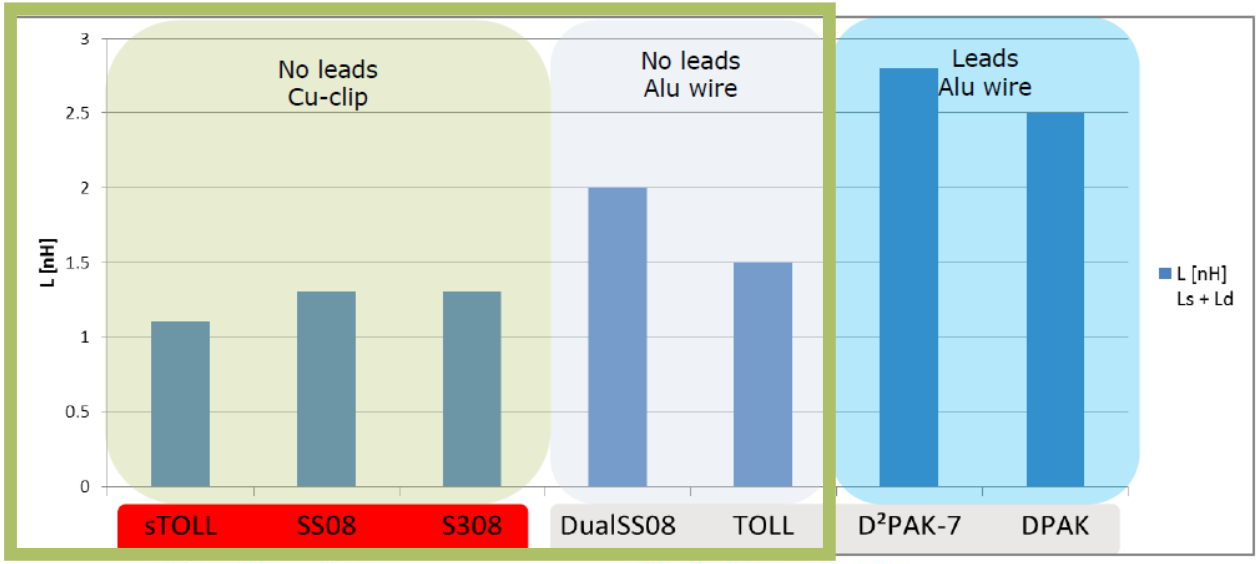
TO262 (I2PAK)

Preliminary Information. Subject to change.
sTOLL registered at JEDEC

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Leadless MOSFETs Interconnect Technology

- **Cu-Clip Packages** offer Lowest Package **Resistance & Inductance**
- Best EMI Behavior
- Lowest Voltage Overshoots







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Robustness of Leadless Packages
IOL Test

IOL=**I**ntermittent **O**perating **L**ivetime („Power Cycling“)

Testing conditions acc. AEC Q101	
Start Temperature	20°C
Temperature rise during cycles	ΔT=100K
Current	Applied to the bodydiode for a few seconds to heat up the chip to the target temperature
Number of tested devices	77
Number of power cycles	15.000 with no failures

Premisses

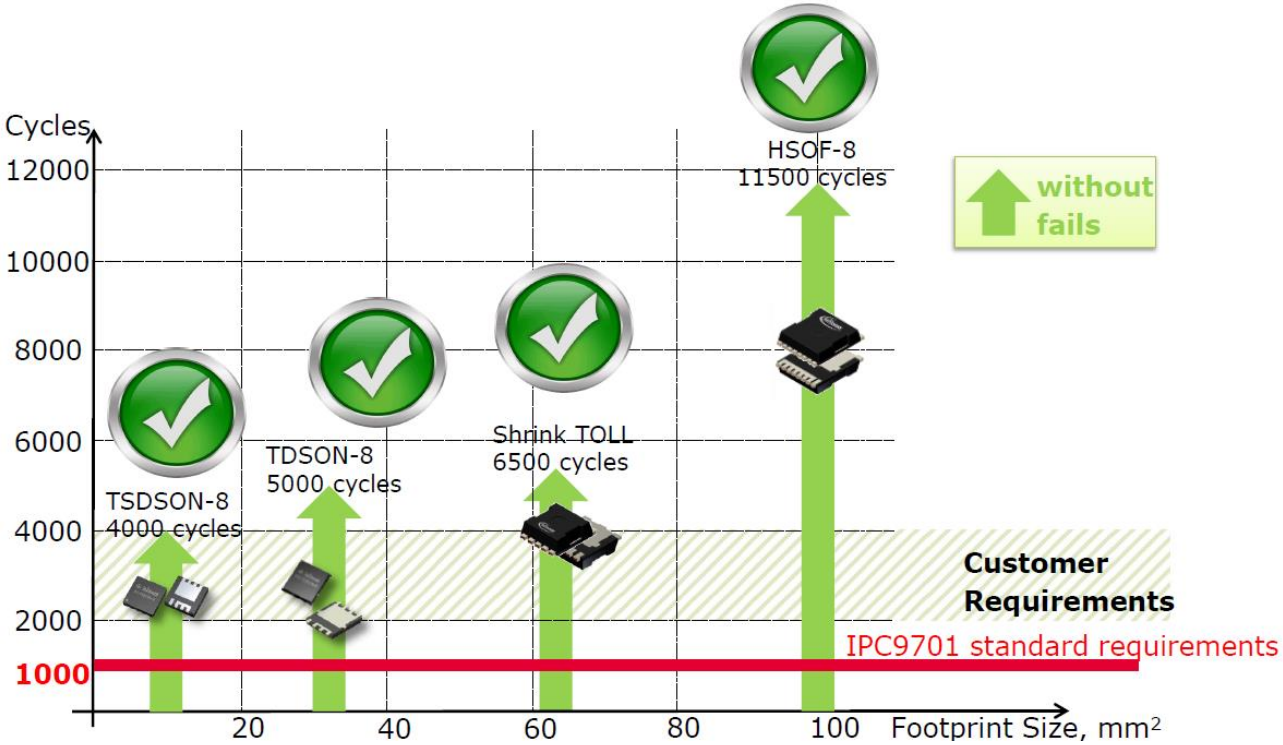
- cooling down the device needs approximately 3 minutes
- a parameter drift of 20% is considered as failure

Measured parameters

All standard parameters according to datasheet:
Leakage currents, V_{BRDSS}, V_{GSth}, $R_{DS(on)}$ etc.

Robustness of Leadless Packages Beyond IPC-9701

› Enhanced TCoB Performance



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80V & 100V MOSFET
Portfolio with Leadless Packages

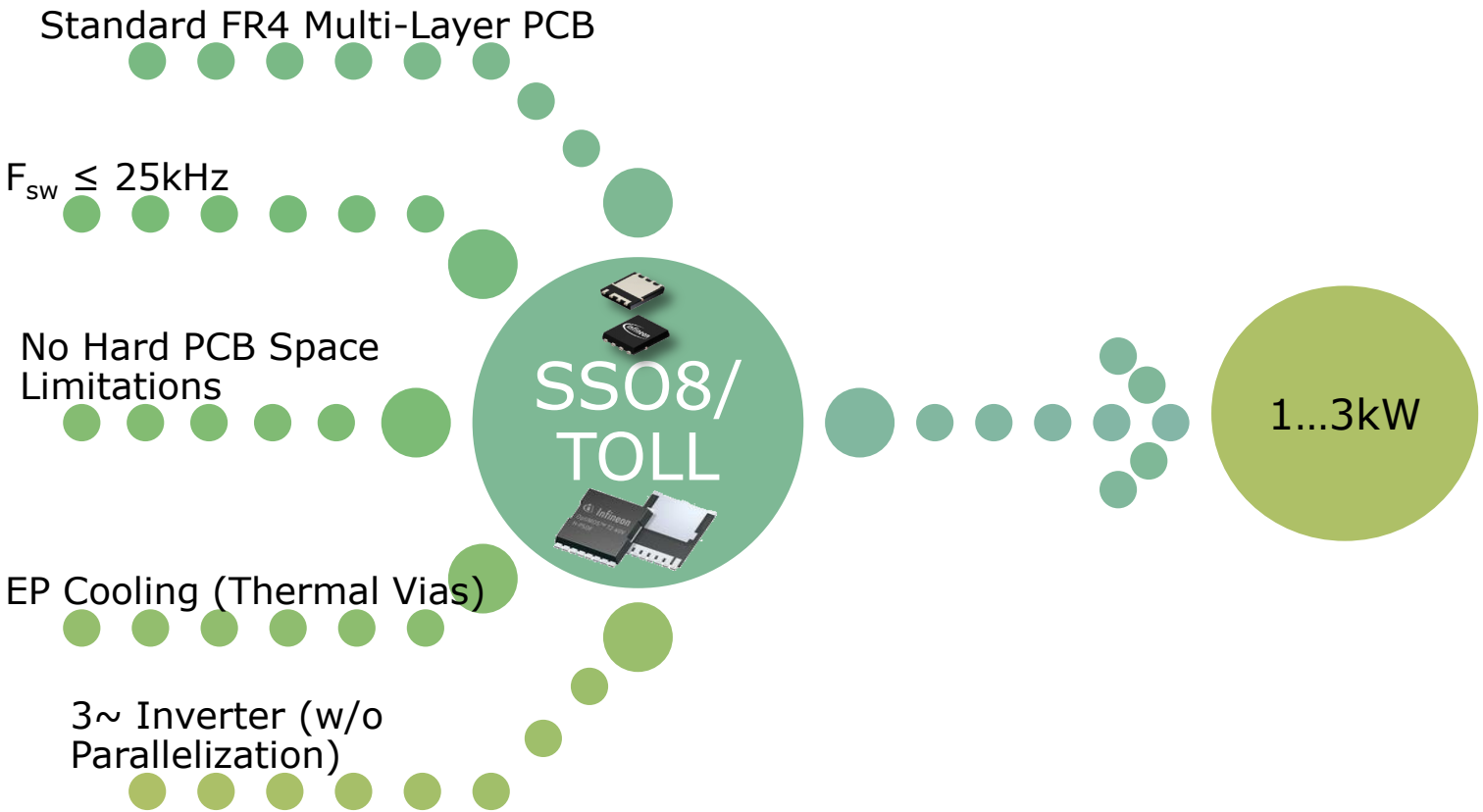
	PQFN 5x6 (TDSON)	PQFN5x6 (TDSON)	SSO8 (TDSON)	SSO8 (TDSON)	TOLL (H-SOF)	TOLL (H-SOF)	DirectFET2 (WDSON)
							
Foot-Print	5x6mm	5x6mm	5x6mm	5x6mm	10x12mm	10x12mm	7x9mm²
I-Package	100A	100A	100A	100A	300A	300A	88A
Released	Gen 10.7 75V	Gen 10.7 100V	OptiMOS™5 80V	OptiMOS™5 100V	OptiMOS™5 80V	OptiMOS™5 100V	Gen10.7 100V
R_{DSon} BiC	*8.5mΩ*	*14.5mΩ*	*3.1mOhm*	*4mOhm*	*1.2mΩ*	*1.5mOhm*	2.8mΩ

- Suitable for standard FR4 PCBs
- High Reliability during TCoB and IOL Tests

Preliminary Information. Subject to change.

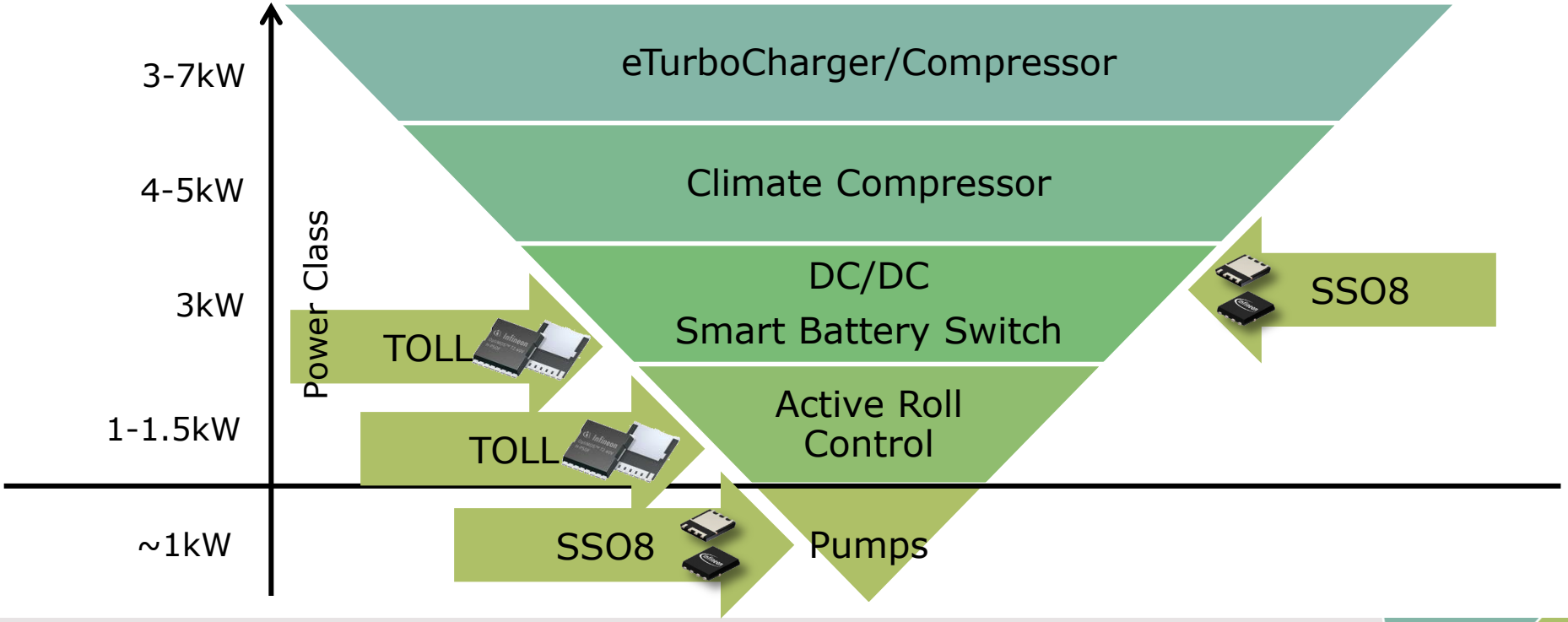
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Limitations of Leadless SMD Packages
System Requirements



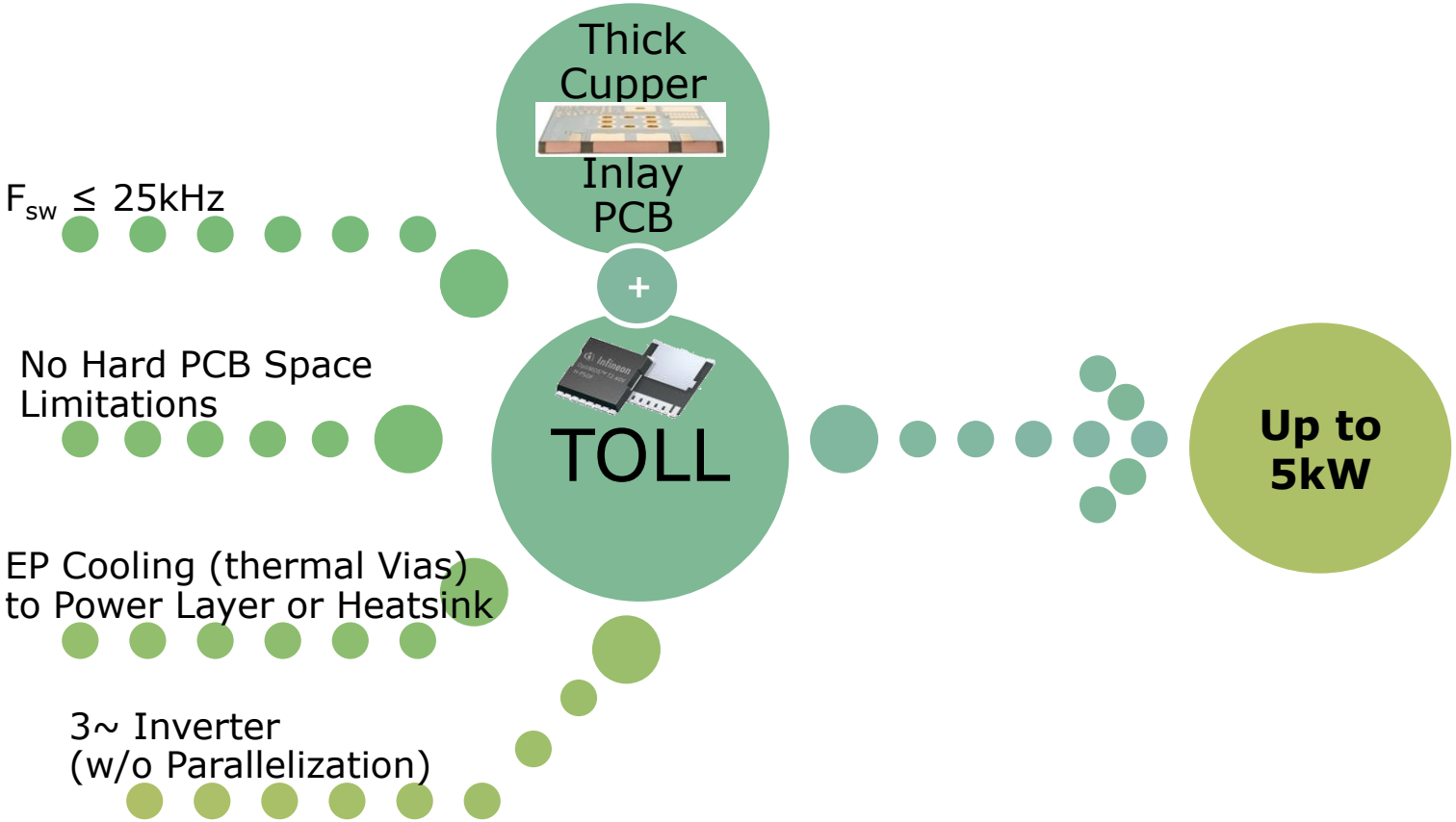
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Leadless SMD MOSFETs
Auxiliary Drives



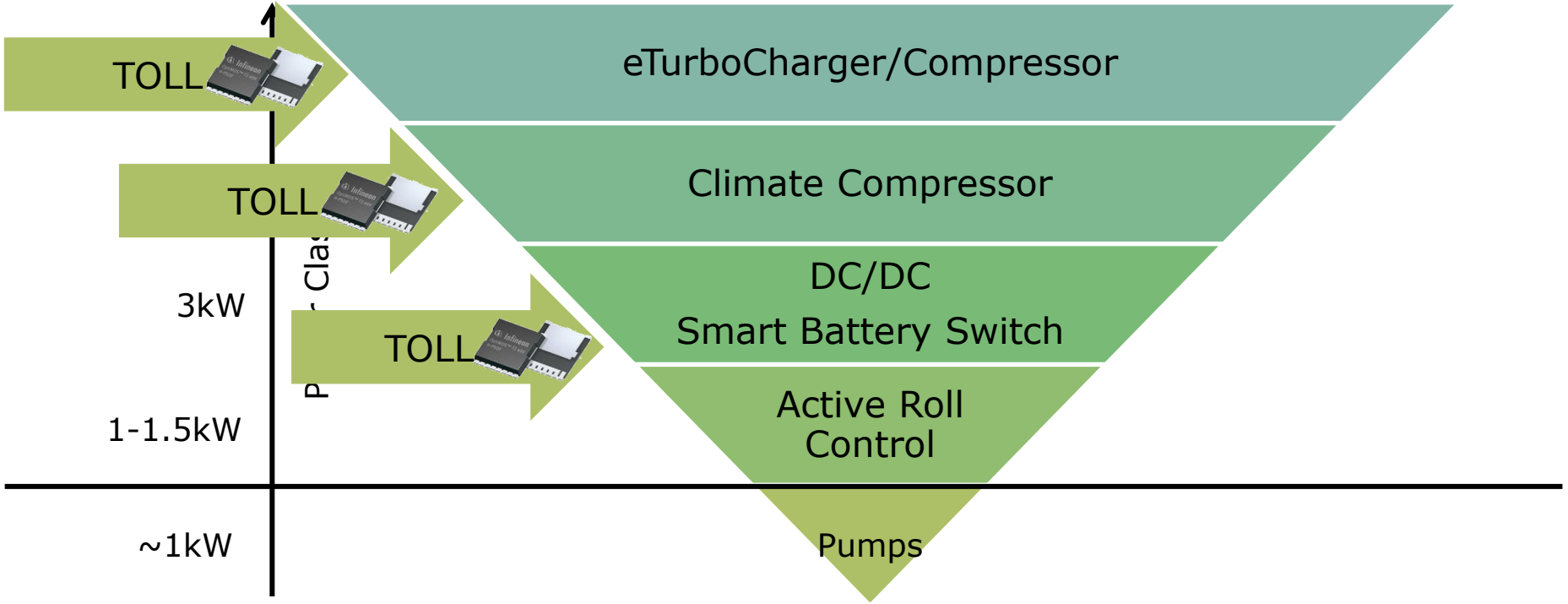
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Limitations of Leadless SMD Packages
Increasing the Output Power with Thick Copper PCB



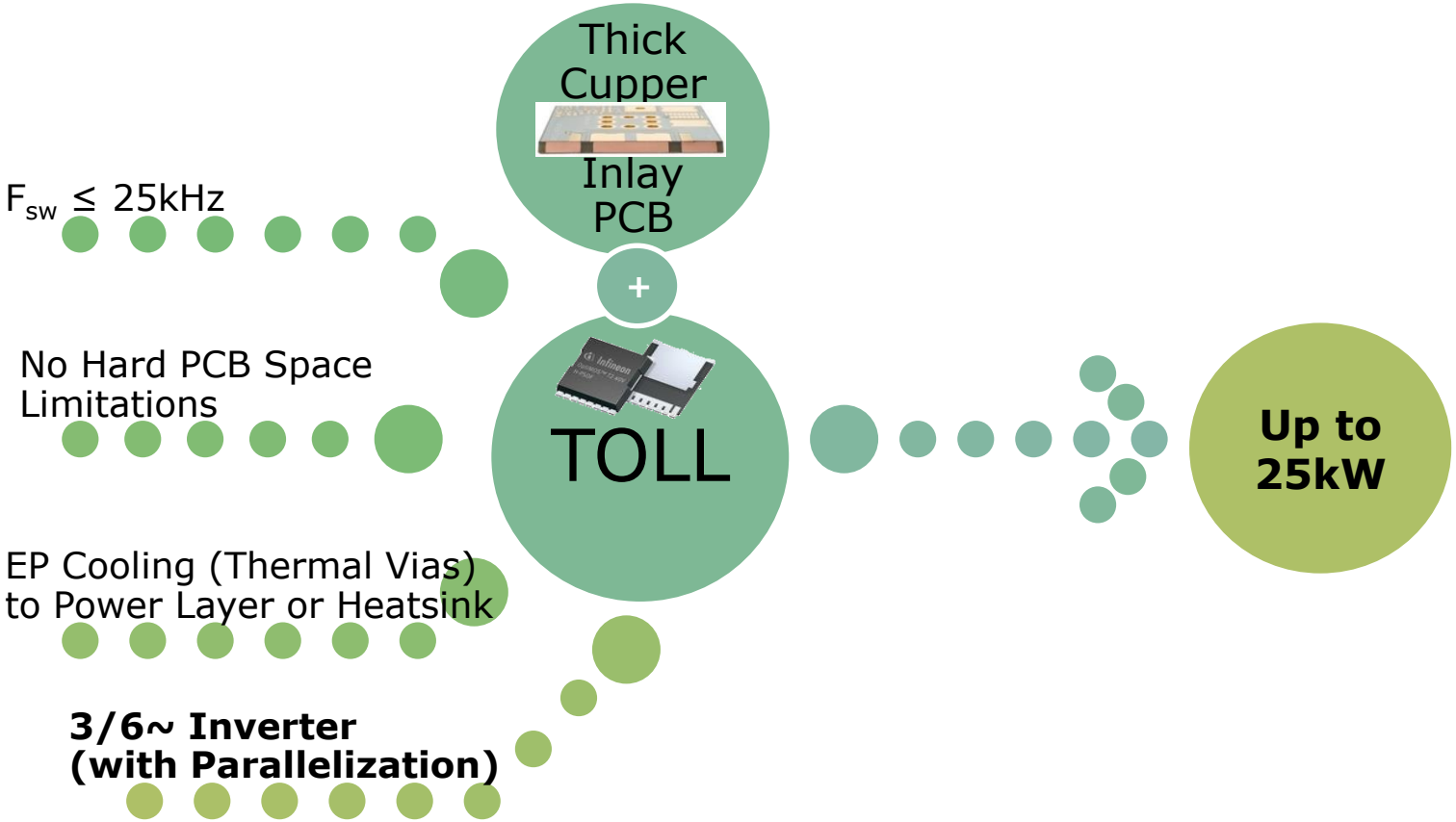
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Leadless SMD MOSFETs
Auxiliary Drives



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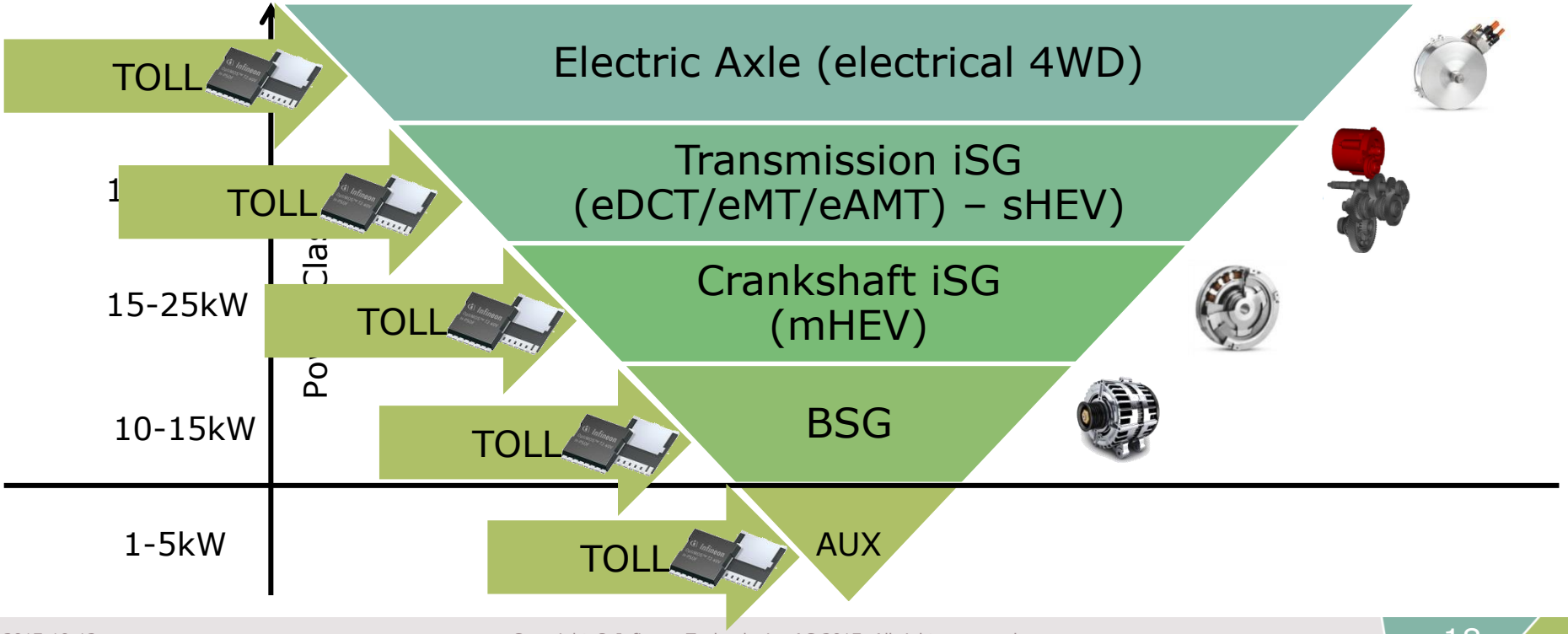
Limitations of Leadless SMD packages
Increasing the Output Power with Thick Copper PCB



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Leadless SMD MOSFETs
High Power Inverters

› Electrification and Hybridization



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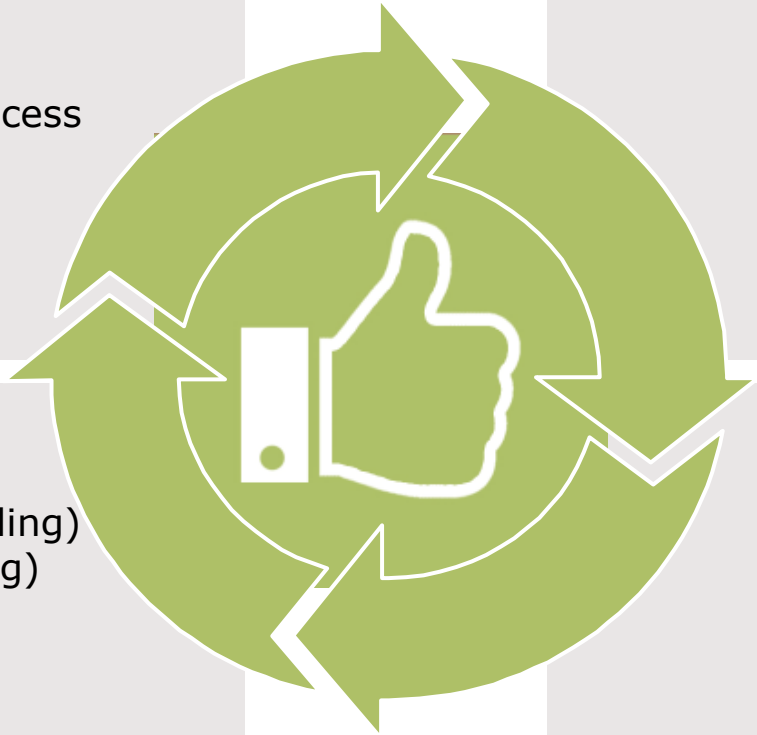
Leadless SMD Packages Advantages

Assembly

- Optical Inspection
- Standard Soldering Process (e.g. Reflow)

Market

- 2nd Source Strategy
- Multiple, Footprint Compatible Alternatives available



Quality

- Fully AECQ qualified
- Proven IOL (Power Cycling) and TCoB (Temp Cycling) Reliability

PCB

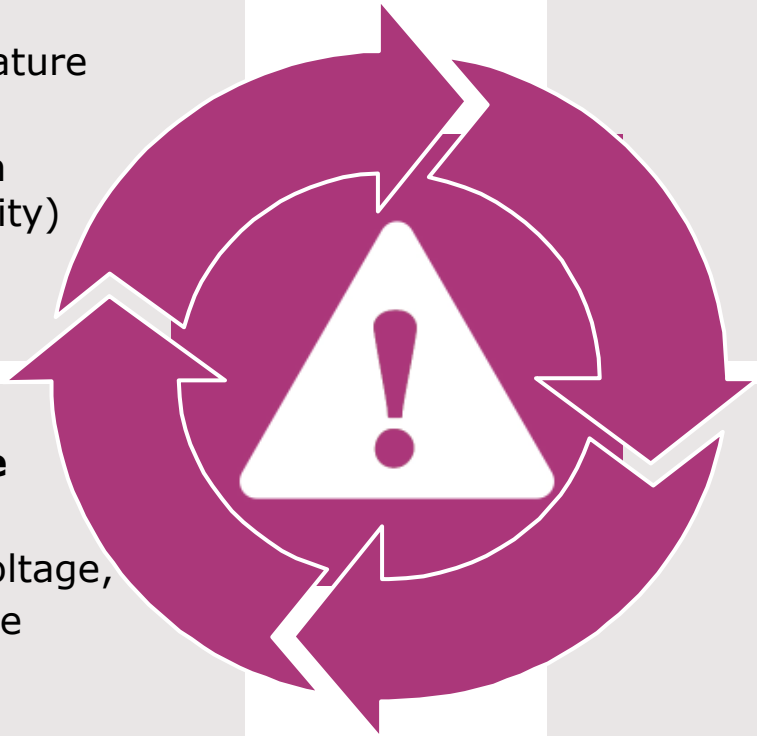
- Standard FR4
- Multiple Supplier
- Well Known Copper Technologies

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Limitations of Leadless SMD Packages
Disadvantages

PCB

- Increased PCB Temperature
- Layout Inflexibility
- High Thermal Stress on Solder Mask (->reliability)
- Only applicable for Copper Substrate



Cooling

- $R_{th\,Junction\text{-}Ambient}$ limited by Package
- Thick Copper Layer or Inlay
- Bottom Side Cooling

Parallel Switching Performance

- Parameter Variation
  - Gate-Threshold Voltage,
  - Breakdown Voltage

Power

- Limited by Bonding/Clipping (per device)

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Agenda

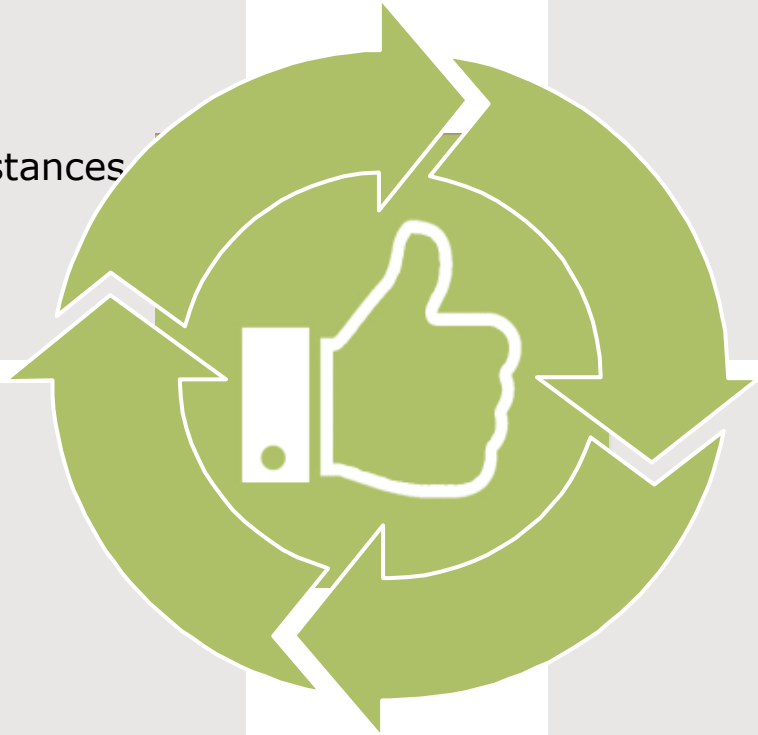
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Bare Dies and MOSFET Modules
Advantages

System Dimensions
- Modules
- Most Flexible Design
- Adaptive to All Circumstances

Power
- Customized Chip Size

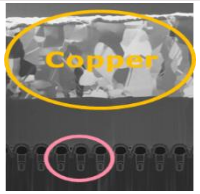


Switching
- Reduced Stray Inductance depending on Design

Temperature & Cooling
- Applicable for HOT Environments (up to 175°C)
- Customized Cooling Approaches
- Homogeneous Power Loss Distribution

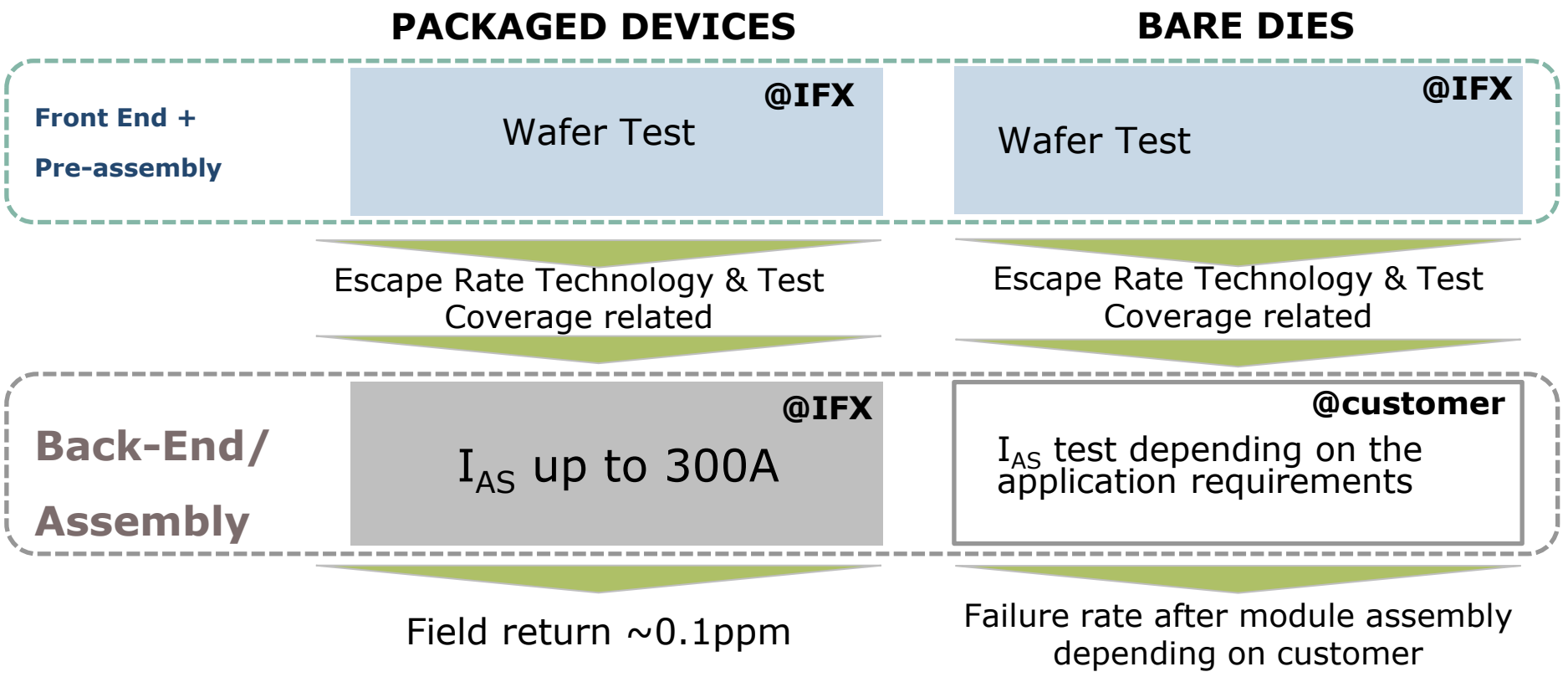
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Bare Dies and MOSFET Modules
Technical Challenges

	Top Metallization	
Handling	Thin Wafer	
	Production Strategy 300mm Wafers	
Quality	Limited Test Coverage in front-end	

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Bare Dies and MOSFET Modules
Reliability: PPM Rates



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Bare Dies and MOSFET Modules
Disadvantages

Yield @ Customer

- Yield Loss after Assembly @ Customer

Handling

- Thin Wafer Technology
- Very sensitive to Cracks
- Strongly depending on Customer's Experience



Testing

- Avalanche Current Testing at Customer Required
- Need of Additional Module Stress Tests (e.g. Power & Temp Cycling)

Assembly

- Customer is Responsible for entire Back-End-of-Line Process

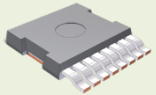
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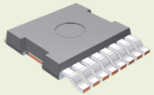
Innovative Packaging Concepts
DirectFET2/TOLG/Top Side Cooling

	DirectFET2 (WDSON)	**TOLG**
		
Foot-Print	7x9	10x12mm
I-Package	88A	300A
Released	Gen10.7 100V	OptiMOS™5 80V
R_{DSon} BiC	*2.8mΩ*	*1.2mΩ*
PCB/Cooling	Dual Side Bottom: FR4 Copper Top: Water Cooling	Bottom Side Bottom: FR4/Al-core IMS

Preliminary Information. Subject to change.

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Innovative Packaging Concepts
TOLG

	DirectFET2 (WDSON)	**TOLG**
		
Foot-Print	7x9	10x12mm
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PCB/Cooling	Dual Side Bottom: FR4 Copper Top: Water Cooling	Bottom Side Bottom: FR4/Al-core IMS

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TOLG
Properties of Al-based IMS and Consequences

› Cu (based Material for the Leadframe of the MOSFET), Al and FR4 have different Coefficients of Thermal Expansion:



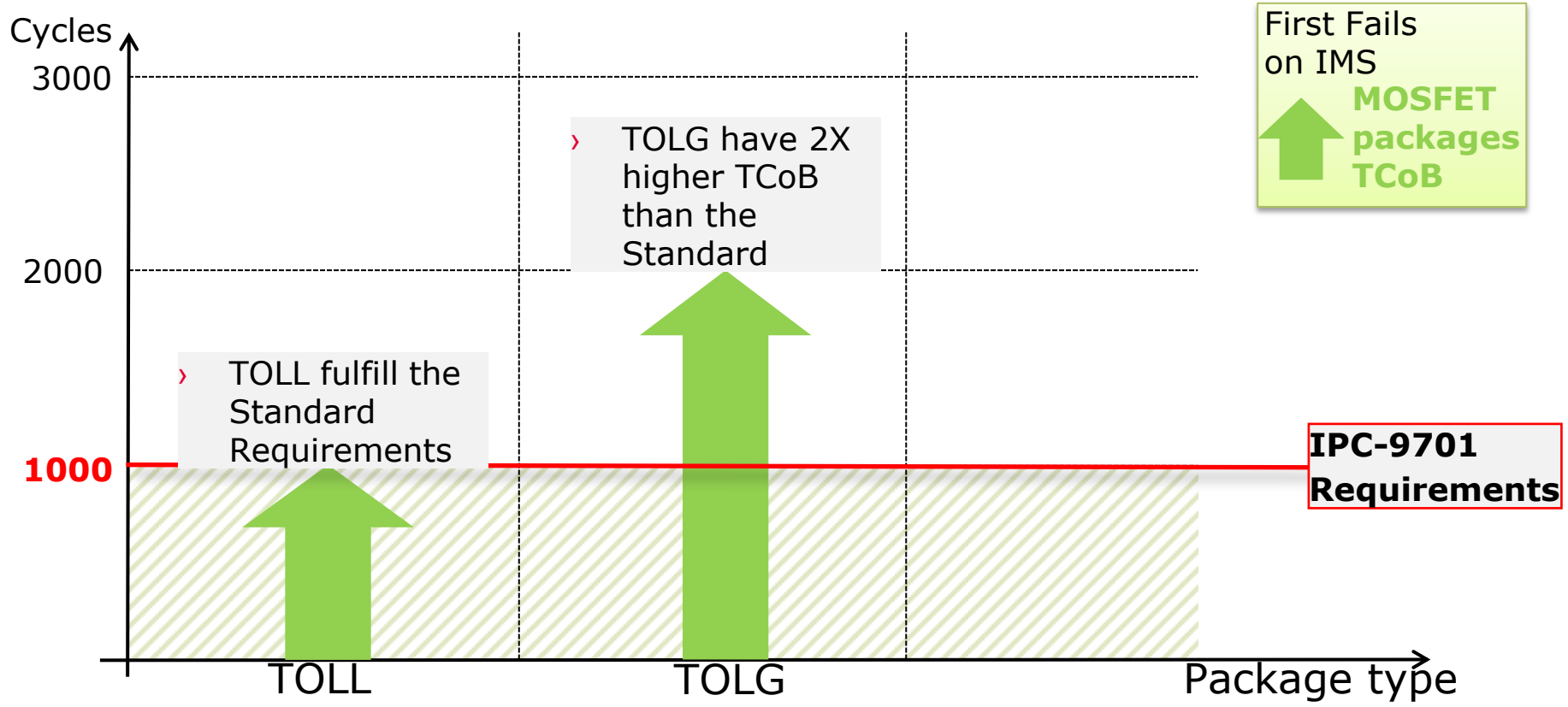
➔ The Mismatch between Cu and Al-Core IMS will lead to higher Stress on the Solder Material, and reduce the Robustness of the System during Thermal Cycles, which may lead to Cracks within the Solder Material

➔ Failure Mode: always Solder Joint Fatigue at the Corner Pins @ Gate/Source

➔ TOLL is appropriate for FR4 Boards and Cu-Core IMS

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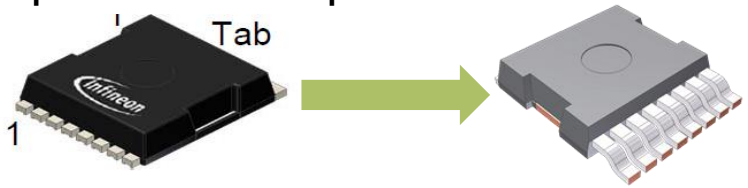
TCoB Performance of TOLL and TOLG on IMS (-40°C to 125°C):



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TOLG
TOLL with Gullwing Geometry

- Infineon investigated a Derivate of the TOLL (TOLL with Gullwing Geometry) to improve TCoB performance on Al-core IMS:



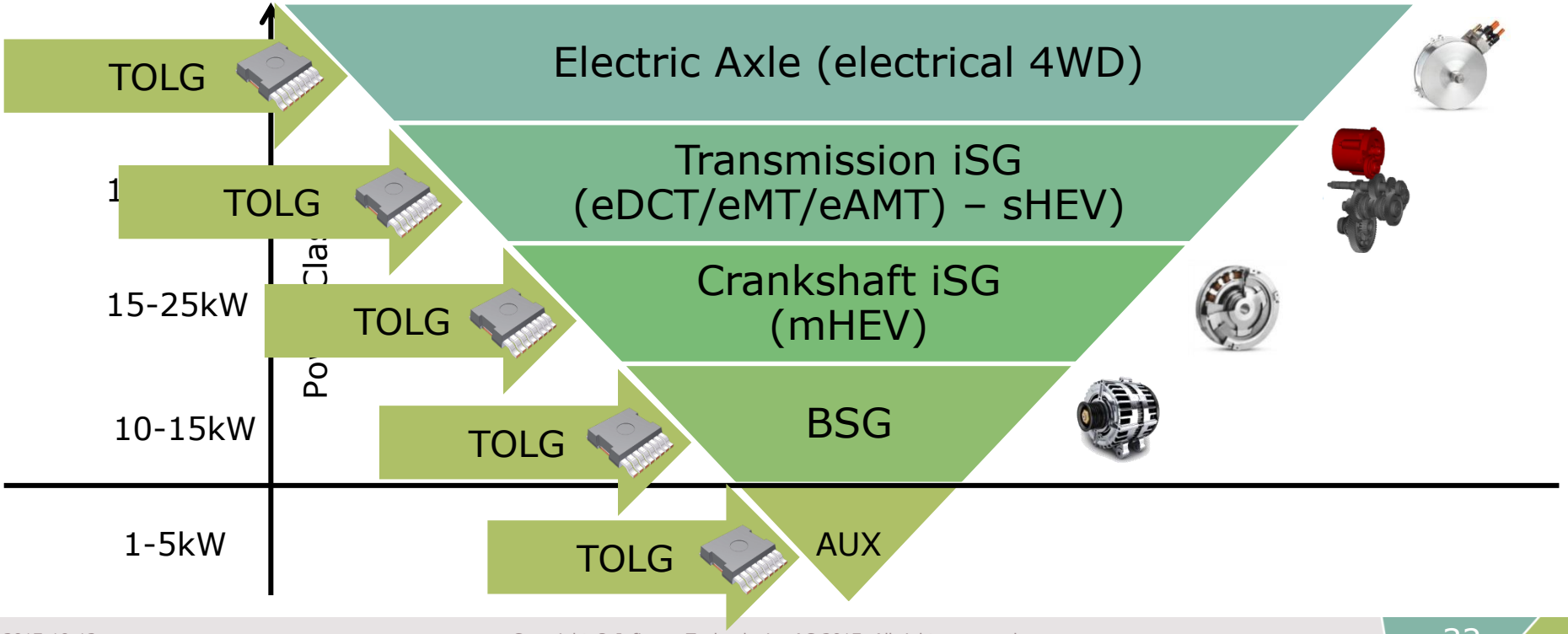
- Results:
  - On IMS: the TOLG performs much better than the TOLL under same Conditions
  - Reason for better Performance is the Flexibility of the Gullwing Leads



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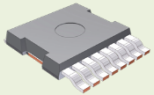
TOLG
High Power Inverters

› Electrification and Hybridization



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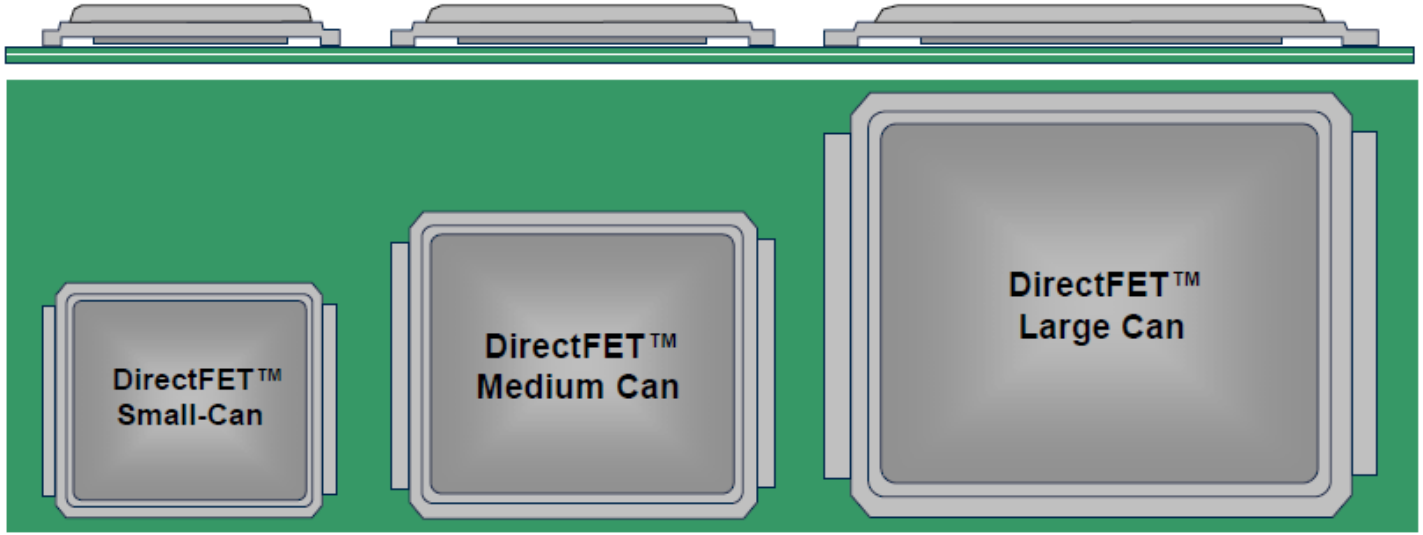
Innovative Packaging Concepts
DirectFET2

	DirectFET2 (WDSON)	**TOLG**
		
Foot-Print	7x9mm	10x12mm
I-Package	88A	300A
Released	Gen10.7 100V	OptiMOS™5 80V
R_{DSon} BiC	*2.8mΩ*	*1.2mΩ*
PCB/Cooling	Dual Side Bottom: FR4 Copper Top: Water Cooling	Bottom Side Bottom: FR4/Al-core IMS

Preliminary Information. Subject to change.

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Innovative Packaging Concepts
DirectFET2



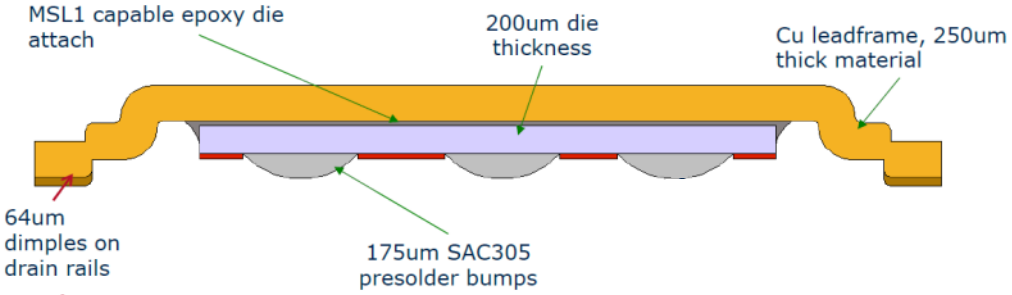
3.95 x 4.85	5.05 x 6.35	7.00 x 9.10
Package: 19.2mm²	**Package: 32.1mm²**	**Package: 63.7mm²**
Max die: 91 x 102mils	**Max die: 133 x 159mils**	**Max die: 220 x 260mils**

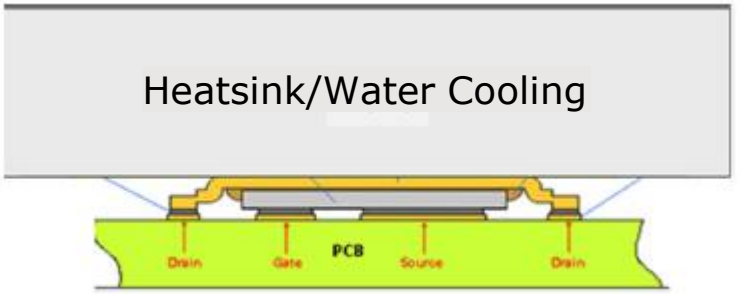
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Innovative Packaging Concepts
DirectFET2

- Allowing Double Side Cooling
  - Top-Side: Heatsink / Water Cooling
  - Bottom-Side: Thermal Vias to Power Cu Layer



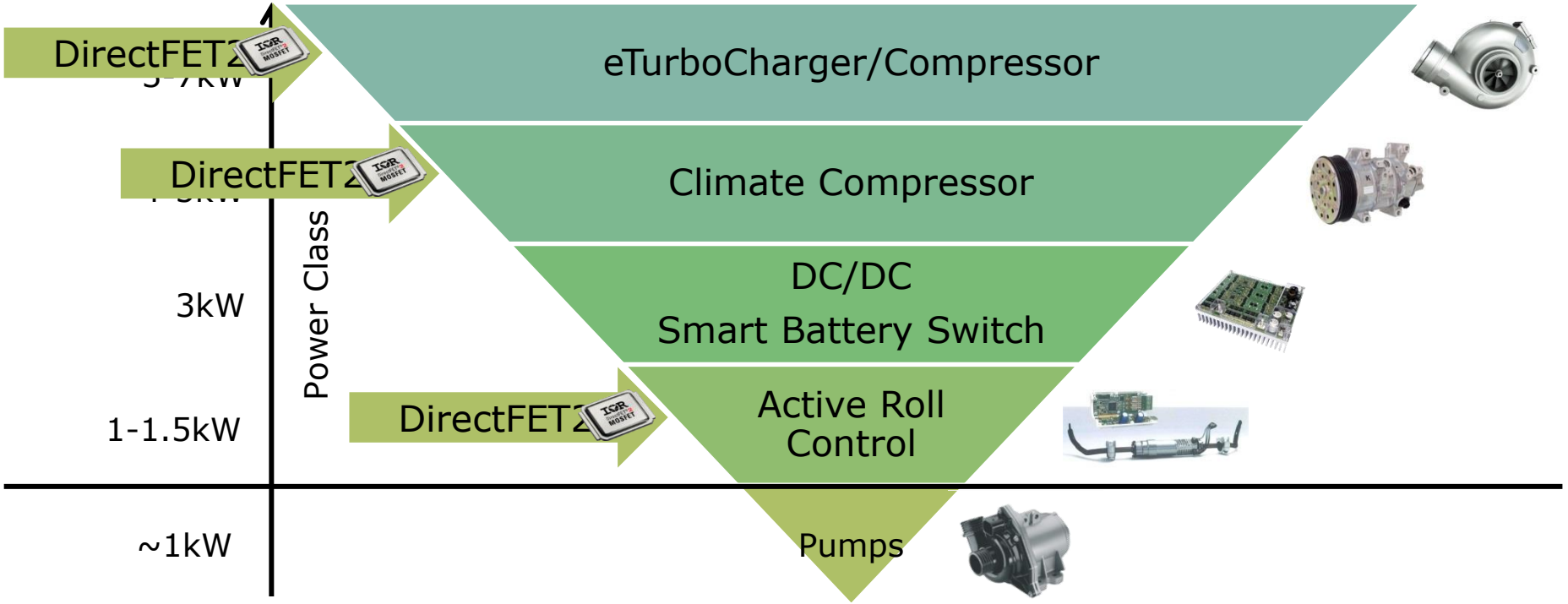




DirectFET2	V_{br}	Rds(on)	Package	R_{th}(JC) Top	Rth(JA) Bottom
AUIRF7669L2	100V	3.5mOhm	Large CAN	0.553 K/W	28.286 K/W
AUIRF7759L2	75V	2.3mOhm	Large CAN	0.881 K/W	26.69 K/W

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DirectFET2 Applications



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DirectFET2 Advantages

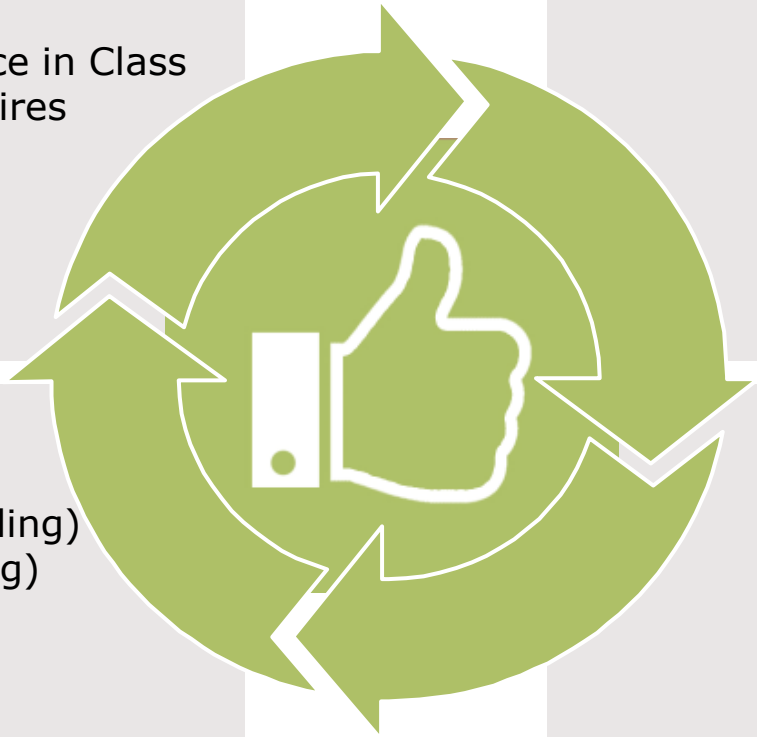
Switching

› Lowest Stray Inductance in Class due to missing Bond Wires

Cooling

› Double Side Cooling

› Very low Top Side R_{th} enables Cooling via CAN to Heatsink



Quality

› Fully AECQ qualified

› Proven IOL (Power Cycling) and TCoB (Temp Cycling) Reliability

PCB

› Standard FR4

› Reduced PCB Temperature

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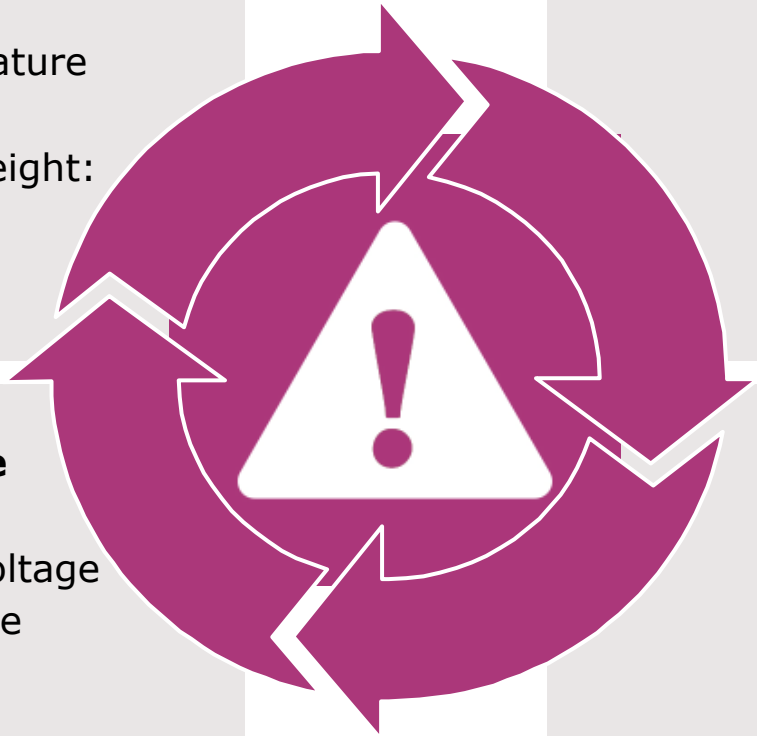
Limitations of DirectFET2 Disadvantages

PCB & Assembly

- Increased PCB Temperature
- Layout Inflexibility
- Deviations of Body's Height: No Homogeneous Placement of Thin Thermal Adhesive

Market

- Unique
- No Footprint Compatible Alternatives



Parallel Switching Performance

- Parameter Variation
  - Gate-Threshold Voltage
  - Breakdown Voltage

Power Cycling

- Bottle Neck : Bottom-Side Solder Bumps (High Thermal Stress)

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Agenda

1. High Power Inverters
2. Leadless SMD Packages
3. Bare Dies and MOSFET Modules
4. Innovative Packaging Concepts
5. Chip Embedding
6. Summary and Outlook

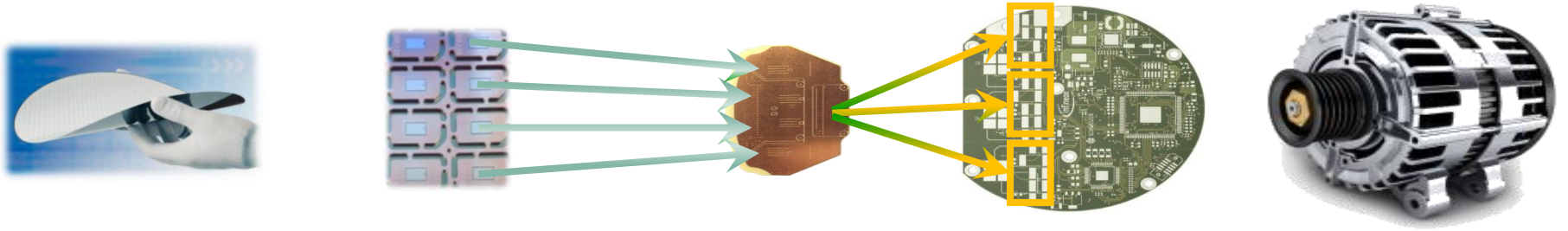
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Chip Embedding
Process Flow

Power MOS Chip Embedding – from Chip to System PCB

SCHWEIZER

Chip | **Standard Cell** | **p²pack** | **Smart p²pack** | **System**



Chip Embedding: Cross Section



Chip Embedding: Increasing System Performance

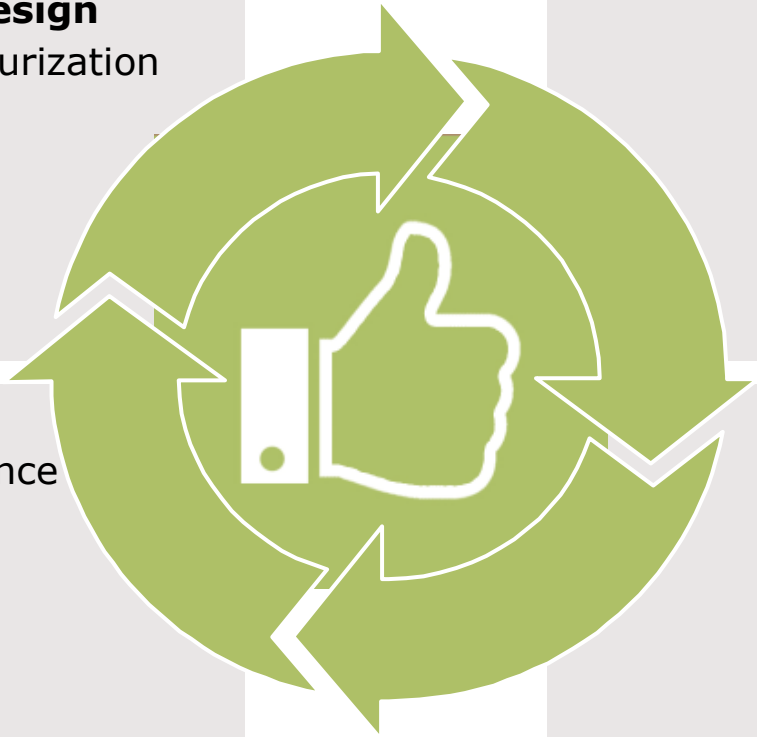
Low Ohmic Conductivity	+++
Low Inductive Switching	+++
System Cooling	+++
System Miniaturization	+++
System Assembly	+++

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Chip Embedding Advantages

System Dimensions/Design
- Compact Design Miniaturization
- PCB Space Savings

Power/Power Losses
- Low $R_{ds}(on)$
- Low R_{th}
- High Power Density

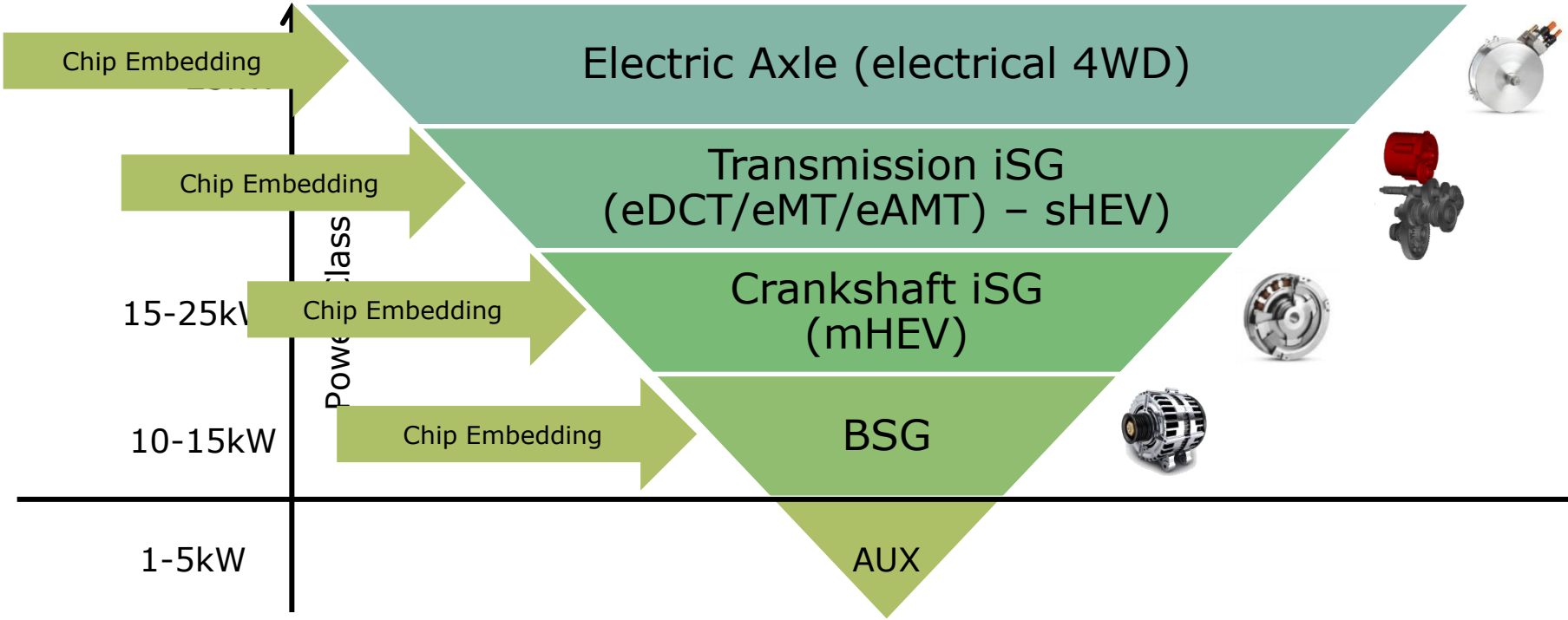


Switching
- Reduced Stray Inductance
- Fast Switching
- Better EMC

Quality
- Increased Reliability

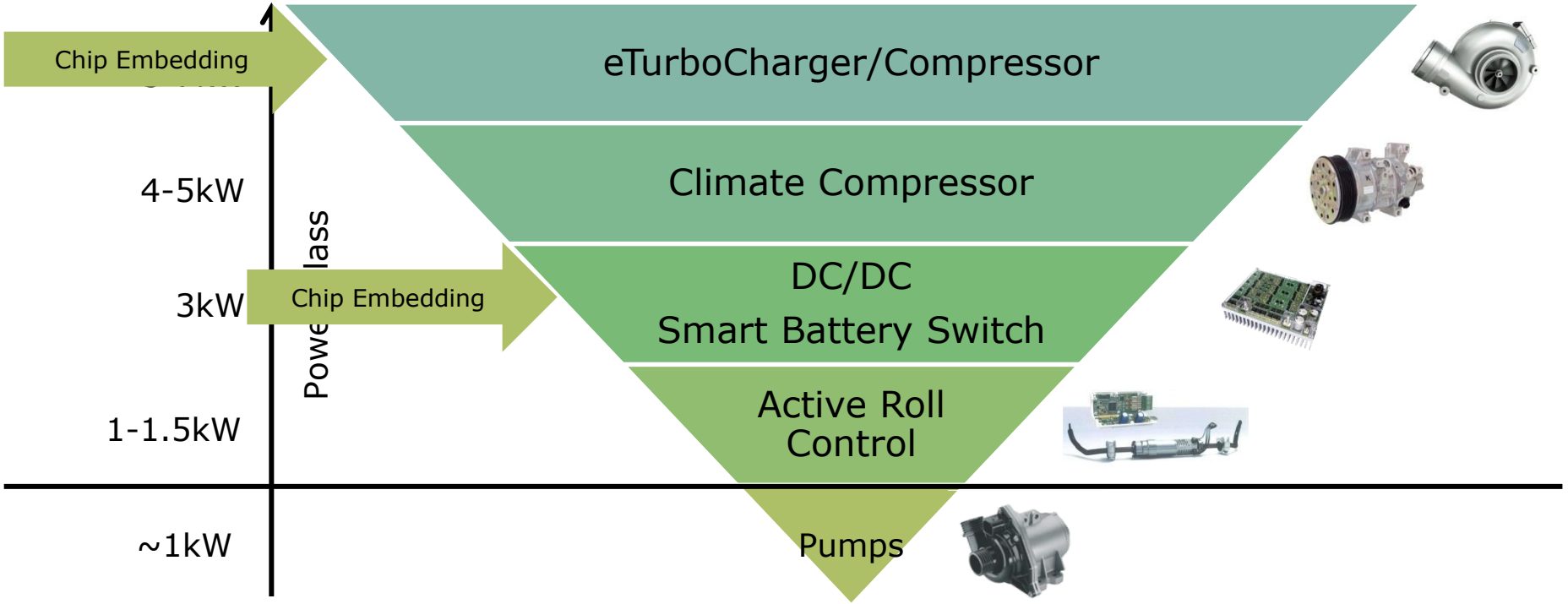
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High Power Inverters
µHybridization



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High Power Inverters
Auxiliary Drives

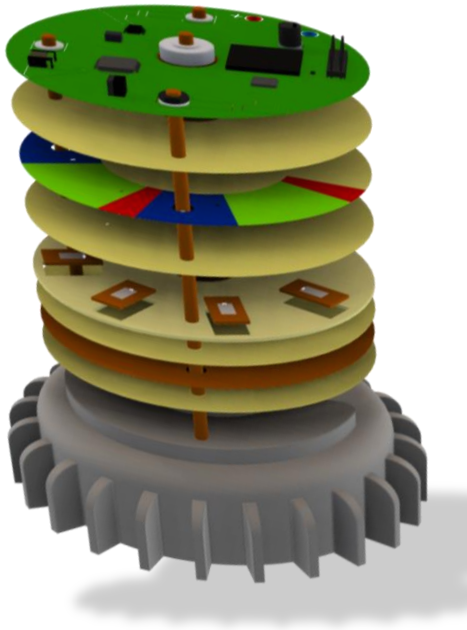


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Power MOS Chip-Embedding
Potential System Improvements & Savings

Ceramic Board or Power PCB + Logic PCB = become only one PCB	→	**Save Connectors and Enhance Interconnects**
Better thermal & electrical Performance	→	**Save Cooling**
Reduction of Chip Size and / or Lower Voltage Class	→	**Save Semiconductor Costs**
Faster Switching possible	→	**Save Passives**
EMC Shielding with Cu-Layers	→	**Save EMC Measures**
Power stages are already insulated	→	**Save Insulator**
Miniaturization - Less Space	→	**Save Room/Space constrains "Money in Hybrid Cars"**
DC Link close to power stages	→	**Save System Costs**

➔ Optimizing System Performance & System Costs



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Comparison Module/CE/Discrete/TOLL-TOLT On Application Level

	Air cooling (**)	External Water Cooling (***)
		TOLL/TOLG on IMS
		(105µmCu, 2mm Al)
RthJH [K/W]		2
R_{thJH} Improvement [%]		-
TJ,max [°C]		175
Ta,max [°C]		110
DT [K]		65
R"pck" [mOhm]		0,16
$R_{"pck"}$ [%]		-
RDSon,max25%C [mOhm]		1,5
$R_{DSon,max"25\%C}$ Improvement [%]		-
Ls [nH]		2
L_s Improvement [%]		-
Switching losses		30%
Max current ratings RMS [A]		95
Current Improvement [%]		-
		Reference:

(*) Concept - based on Simulation
(**) Low Budget Cooling
(***) High End Cooling

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Comparison Module/CE/Discrete/TOLL-TOLT On Application Level

	Air cooling (**)	External Water Cooling (***)
	DCB	**TOLL/TOLG on IMS**
	Wedge bonded 175µm Si	(105µmCu, 2mm Al)
RthJH [K/W]	2	2
R_{thJH} Improvement [%]	0%	-
TJ,max [°C]	175	175
Ta,max [°C]	110	110
DT [K]	65	65
R"pck" [mOhm]	0,5	0,16
$R_{"pck"}$ [%]	213%	-
RDSon,max25%C [mOhm]	1,84	1,5
$R_{DSon,max"25\%C}$ Improvement [%]	23%	-
Ls [nH]	5	2
L_s Improvement [%]	150%	-
Switching losses	40%	30%
Max current ratings RMS [A]	84	95
Current Improvement [%]	-12%	-
		Reference:

(*) Concept - based on Simulation
(**) Low Budget Cooling
(***) High End Cooling

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Comparison Module/CE/Discrete/TOLL-TOLT On Application Level

	Air cooling (**)	External Water Cooling (***)	
	DCB	**DCB**	**TOLL/TOLG on IMS**
	Wedge bonded 175µm Si	Wedge bonded 175µm Si	(105µmCu, 2mm Al)
RthJH [K/W]	2	1	2
R_{thJH} Improvement [%]	0%	-50%	-
TJ,max [°C]	175	175	175
Ta,max [°C]	110	110	110
DT [K]	65	65	65
R"pck" [mOhm]	0,5	0,5	0,16
$R_{"pck"}$ [%]	213%	213%	-
RDSon,max25%C [mOhm]	1,84	1,84	1,5
$R_{DSon,max"25\%C}$ Improvement [%]	23%	23%	-
Ls [nH]	5	5	2
L_s Improvement [%]	150%	150%	-
Switching losses	40%	40%	30%
Max current ratings RMS [A]	84	117	95
Current Improvement [%]	-12%	23%	-
			Reference:

(*) Concept - based on Simulation
(**) Low Budget Cooling
(***) High End Cooling

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Comparison Module/CE/Discrete/TOLL-TOLT On Application Level

	Air cooling (**)	External Water Cooling (***)		
	DCB	**DCB**	**DCB (*)**	**TOLL/TOLG on IMS**
	Wedge bonded 175µm Si	Wedge bonded 175µm Si	SFS 70µm Si	(105µmCu, 2mm Al)
RthJH [K/W]	2	1	0,9	2
R_{thJH} Improvement [%]	0%	-50%	-55%	-
TJ,max [°C]	175	175	175	175
Ta,max [°C]	110	110	110	110
DT [K]	65	65	65	65
R"pck" [mOhm]	0,5	0,5	0,12	0,16
$R_{"pck"}$ [%]	213%	213%	-25%	-
RDSon,max25%C [mOhm]	1,84	1,84	1,46	1,5
$R_{DSon,max"25\%C}$ Improvement [%]	23%	23%	-3%	-
Ls [nH]	5	5	2	2
L_s Improvement [%]	150%	150%	0%	-
Switching losses	40%	40%	30%	30%
Max current ratings RMS [A]	84	117	144	95
Current Improvement [%]	-12%	23%	52%	-
				Reference:

(*) Concept - based on Simulation
(**) Low Budget Cooling
(***) High End Cooling

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Comparison Module/CE/Discrete/TOLL-TOLT On Application Level

	Air cooling (**)	External Water Cooling (***)			
	DCB	**DCB**	**DCB (*)**	**TOLL/TOLG on IMS**	**CE (*)**
	Wedge bonded 175µm Si	Wedge bonded 175µm Si	SFS 70µm Si	(105µmCu, 2mm Al)	
RthJH [K/W]	2	1	0,9	2	1
R_{thJH} Improvement [%]	0%	-50%	-55%	-	-50%
TJ,max [°C]	175	175	175	175	175
Ta,max [°C]	110	110	110	110	110
DT [K]	65	65	65	65	65
R"pck" [mOhm]	0,5	0,5	0,12	0,16	0,1
$R_{"pck"}$ [%]	213%	213%	-25%	-	-38%
RDSon,max25%C [mOhm]	1,84	1,84	1,46	1,5	1,44
$R_{DSon,max"25\%C}$ Improvement [%]	23%	23%	-3%	-	-4%
Ls [nH]	5	5	2	2	"1"
L_s Improvement [%]	150%	150%	0%	-	-50%
Switching losses	40%	40%	30%	30%	20%
Max current ratings RMS [A]	84	117	144	95	144
Current Improvement [%]	-12%	23%	52%	-	52%
				Reference:	

(*) Concept - based on Simulation
(**) Low Budget Cooling
(***) High End Cooling

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Comparison Module/CE/Discrete/TOLL-TOLT On Application Level

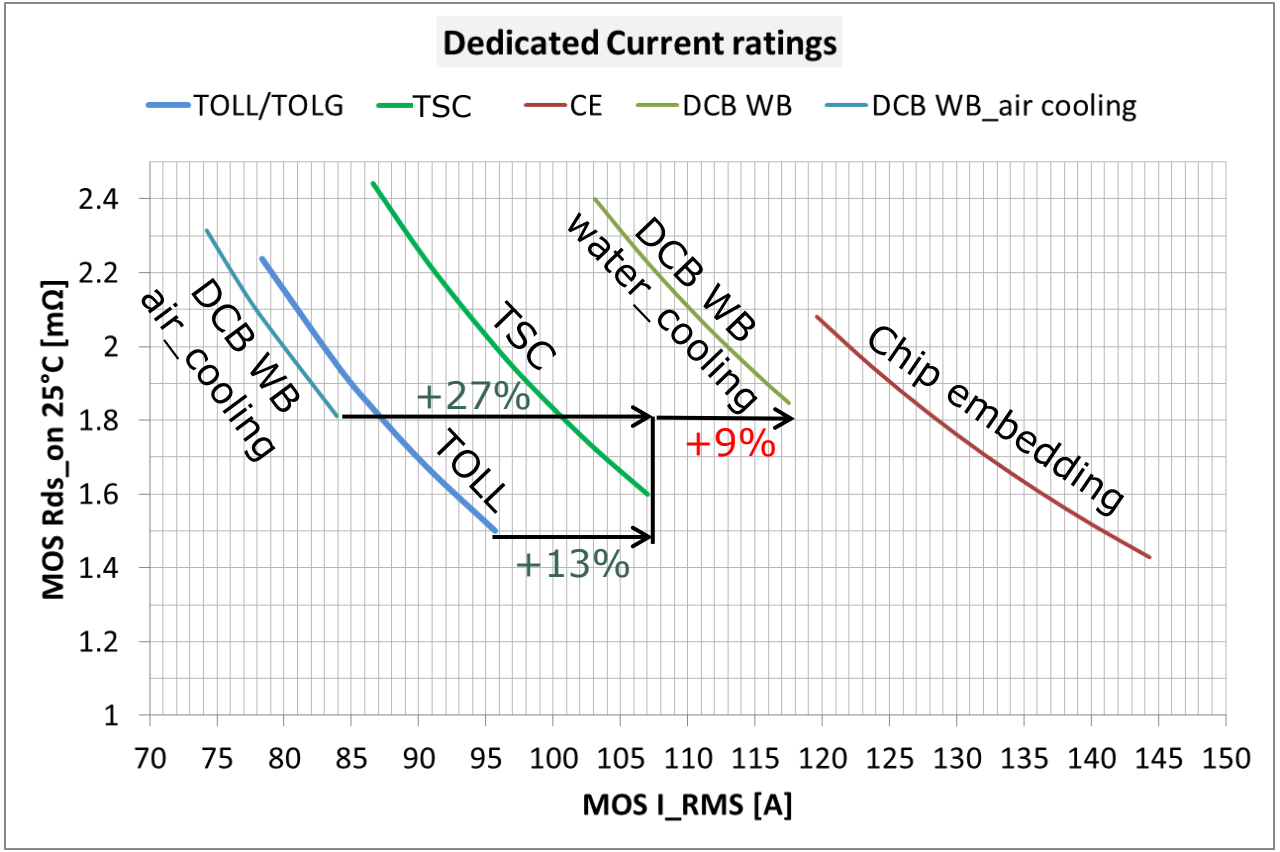
	Air cooling (**)	External Water Cooling (***)				
	DCB	**DCB**	**DCB (*)**	**TOLL/TOLG on IMS**	**CE (*)**	**Top Side Cooling (*)**
	Wedge bonded 175µm Si	Wedge bonded 175µm Si	SFS 70µm Si	(105µmCu, 2mm Al)		
RthJH [K/W]	2	1	0,9	2	1	1,6
R_{thJH} Improvement [%]	0%	-50%	-55%	-	-50%	-20%
TJ,max [°C]	175	175	175	175	175	175
Ta,max [°C]	110	110	110	110	110	110
DT [K]	65	65	65	65	65	65
R"pck" [mOhm]	0,5	0,5	0,12	0,16	0,1	0,16
$R_{"pck"}$ [%]	213%	213%	-25%	-	-38%	0%
RDSon,max25%C [mOhm]	1,84	1,84	1,46	1,5	1,44	1,5
$R_{DSon,max"25\%C}$ Improvement [%]	23%	23%	-3%	-	-4%	0%
Ls [nH]	5	5	2	2	"1"	2
L_s Improvement [%]	150%	150%	0%	-	-50%	0%
Switching losses	40%	40%	30%	30%	20%	30%
Max current ratings RMS [A]	84	117	144	95	144	107
Current Improvement [%]	-12%	23%	52%	-	52%	13%
				Reference:		

(*) Concept - based on Simulation
(**) Low Budget Cooling
(***) High End Cooling

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Current Ratings Distribution According to Packages and Cooling Concept

- 100V MOS $R_{ds}(on)$@25C Vs Id_RMS (Application Verification)



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Summary
Comparison of MOSFET Solutions

	TOLL TOLG	**DirectFET2**	**Bare Die (Modules)**	**Chip Embedding (P²PAK)**
Technology	SFET5 ++	Gen10.7 +	SFET4 +	SFET5 ++
BiC Rds(on)	1.5mOhm (100V) 1.2mOhm (80V)	2.8mOhm (100V) 1.8mOhm (75V)	1.9mOhm (100V) 0.66mOhm (80V)	flexible
Space Consumption (based on 15kW 3 phase inverter)	4x 6 MOSFETs = 24 2880mm² 0	4x 6 MOSFETs = 24 1560mm² +	30.24mm²/die * 2 (in parallel) * 6 = 362.88mm² (die space) + module -	30mm² / chip P²PAK can be integrated space-neutral (embedding) ++
Costs	+	+	-	--
Product Current (Single Chip)	300A +	124A -	272A 0	300A +

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Summary
Comparison of MOSFET Solutions

	TOLL TOLG	DirectFET2	Bare Die (Modules)	Chip Embedding (P²PAK)
Customization: differentiation to the competition	-	+	++	++
Layout flexibility	0	0	++	++
Handling	+	0	-	0
Portability from one gen to the next	++	0	-	++ (TIER1)

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